What is claimed is:

1. An integrated circuit (IC) supporting non-electrically-programmable three-dimensional memory (NEP-3DM)-based self-test (NEP-3DMST), comprising

a substrate circuit, said substrate circuit further comprising a circuit-under-test (CUT) and a peripheral circuit; and,

at least an NEP-3DM level stacked on said substrate circuit, at least a portion of said NEP-3DM level storing at least a portion of test data and/or test-data seeds for said CUT and being connected with said peripheral circuit through a plurality of inter-level connecting vias.

2. The IC supporting NEP-3DMST according to claim 1, wherein said substrate circuit further comprises a plurality of test-vector buffers, said test-vector buffers storing at least a portion of said test data and/or test-data seeds.

3. The IC supporting NEP-3DMST according to claim 1, wherein said test data or test-data seeds are downloaded into said CUT in a serial fashion.

4. The IC supporting NEP-3DMST according to claim 1, wherein said test data or test-data seeds are downloaded into said CUT in a parallel fashion.

5. The IC supporting NEP-3DMST according to claim 1, wherein

said CUT comprises a first CUT block and a second CUT block;

said substrate circuit further comprises a first test-vector buffer and a second test-vector buffer, said first test-vector buffer storing at least a portion of test data and/or test-data seeds for said first CUT block, said second test-vector buffer storing at least a portion of test data and/or test-data seeds for said second CUT block.

6. The IC supporting NEP-3DMST according to claim 1, wherein said substrate circuit further comprises a D/A converter, said D/A converter converting at least a portion of said digital test vectors into analog signals.

7. The IC supporting NEP-3DMST according to claim 6, wherein said substrate circuit further comprises an analog comparator.

8. The IC supporting NEP-3DMST according to claim 1, wherein

said test data and/or test-data seeds in said NEP-3DM are compressed test data;

said substrate circuit further comprises a data de-compressor, said data de-compressor de-compressing said compress test data.

9. The IC supporting NEP-3DMST according to claim 1, wherein

said test data and/or test-data seeds in said NEP-3DM are compressed test data;

said substrate circuit further comprises a data compressor, said data compressor compressing output test vectors.

10. The IC supporting NEP-3DMST according to claim 1, wherein said substrate circuit further comprises a storage block, said storage block storing address information associated with mismatched output test vectors and expected test vectors.

11. The IC supporting NEP-3DMST according to claim 1, wherein said substrate circuit further comprises a multiplexor, the output of said multiplexor being selected from external scan-test input and NEP-3DM input.

12. The IC supporting NEP-3DMST according to claim 1, wherein said substrate circuit further comprises a plurality of parallel-serial test flip-flops (PS-TFF), the output of said PS-TFF being selected from normal data input, external scan-test input, and NEP-3DM input.

13. A process of testing an circuit-under-test (CUT) having a non-electrically-programmable three-dimensional memory (NEP-3DM) stacked thereon, comprising the steps of:

(A) reading input test vectors and expected test vectors from said NEP-3DM ;

(B) sending said input test vectors to said CUT and getting output test vectors;

(C) comparing said output test vectors with said expected test vectors.

14. The process according to claim 13, further comprising the step of built-in self-test (BIST) to said CUT.

15. The process according to claim 13, further comprising the step of external scan-test (EST) to said CUT.

16. The process according to claim 14, wherein

said EST is performed after said step (C); and

said EST is only performed to test vectors associated with mismatched output test vectors and expected test vectors.

17. The process according to claim 13, further comprising the step of testing and correcting said EP-3DM before said step (A).

18. A printed-circuit-board-under-test (PCB-UT), comprising at least a first integrated circuit (IC) chip, said first IC chip further comprising a non-electrically-programmable three-dimensional memory (NEP-3DM), said NEP-3DM storing at least of a portion of test data and/or test-data seeds for at least a portion of said PCB-UT.

19. The PCB-UT according to claim 18, further comprising a test interface, whereby said NEP-3DM can be tested through said test interface.

20. The PCB-UT according to claim 18, further comprising a second IC chip, the test data and/or test-data seeds for said second IC chip being stored in said NEP-3DM on said first IC chip.